

66200T-8T05F460

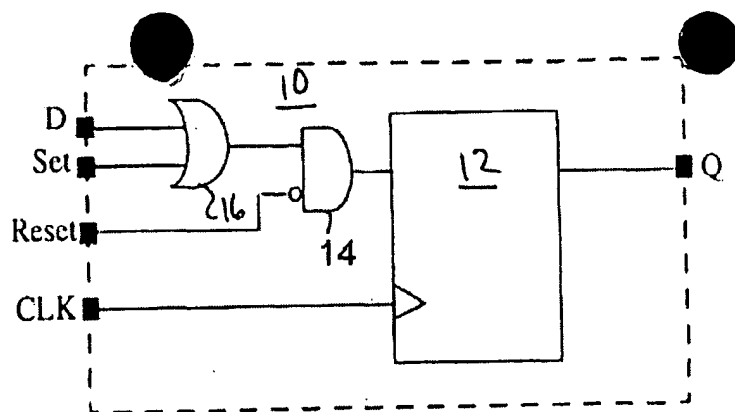


FIG. 1

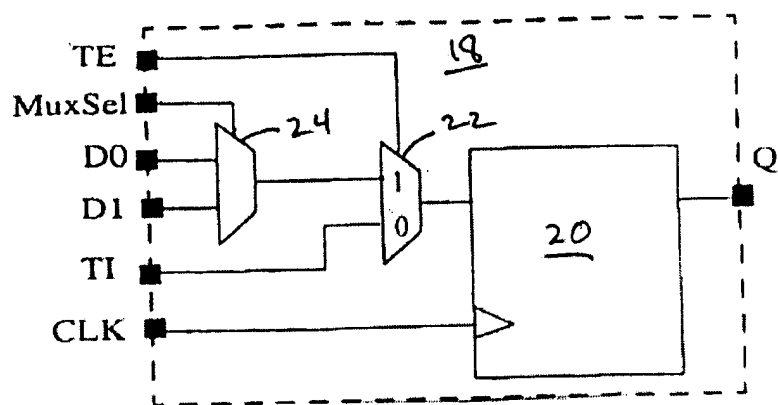


FIG. 2

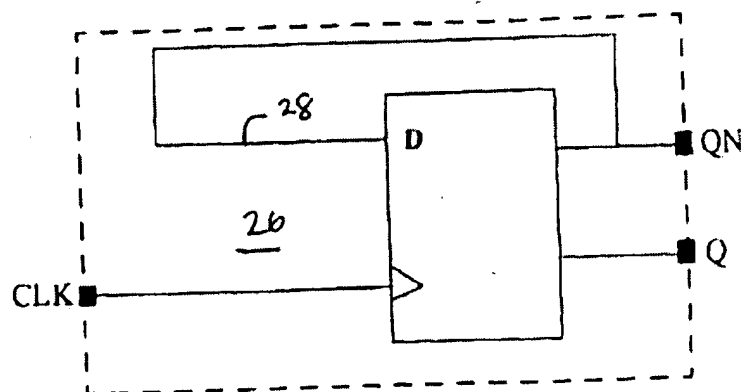


FIG. 3

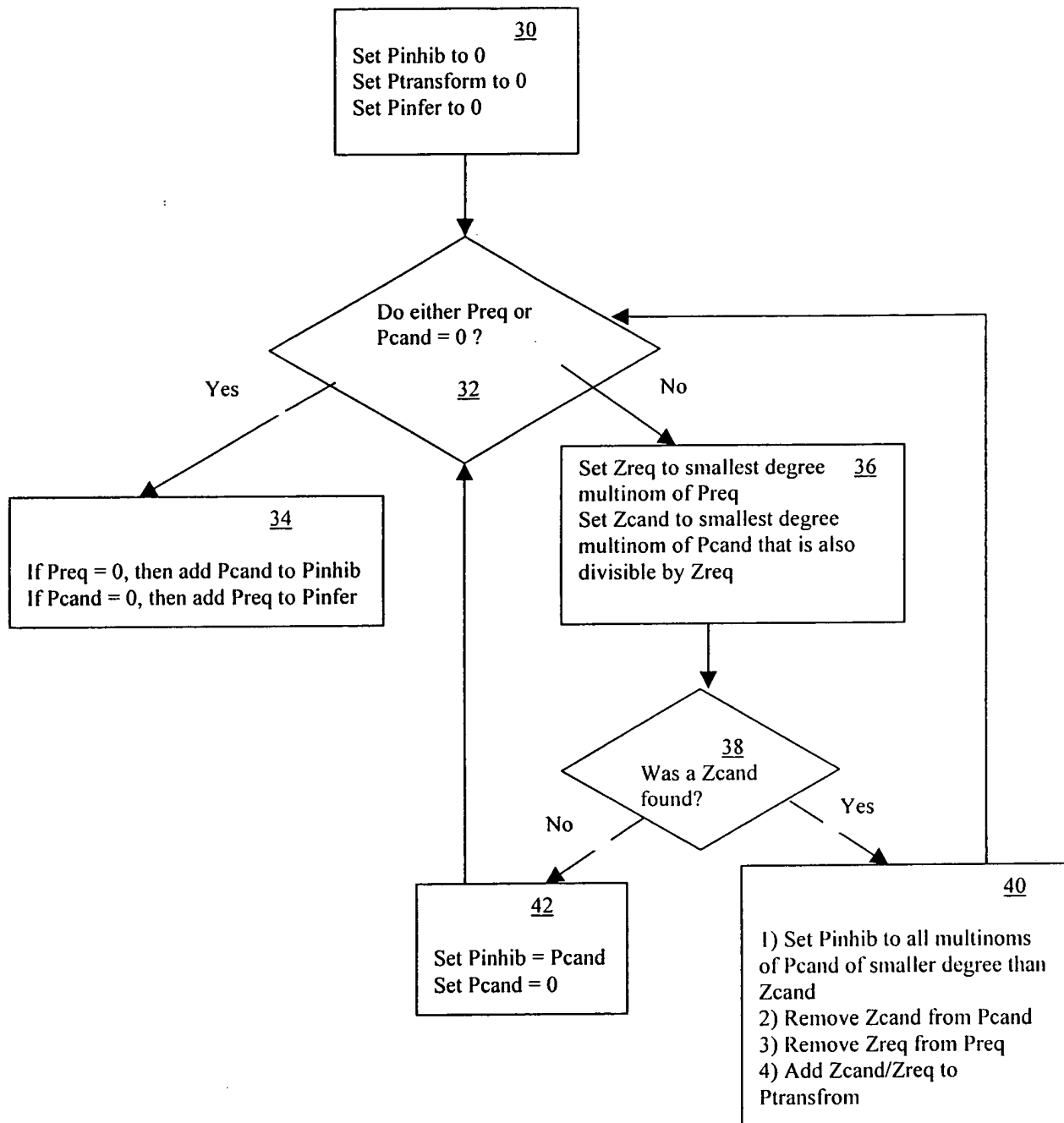


FIG. 4

09415018-10099

Inhibition	
Rst	inhib a Reset active high
RstLr	inhib a Reset active low
St	inhib a Set active high
StLs	inhib a Set active low
ScStRst	inhib a Scan active high
ScStLsRstLc	inhib a Scan active low
MuScStRst	inhib a Mux
Re	inhib a Recirculating active high
ReLre	inhib a Recirculating active low
T	stop proces, impossible to inhib a Toggle element

FIG. 5

Transformation	
rule 1	1: Do nothing
rule 2	Ls or Ls⁻¹: Add an inverter on the Reset terminal
rule 3	Lr or Lr⁻¹: Add an inverter on the Set terminal
rule 4	Lre or Lre⁻¹: Add an inverter on the Recirculating enable
rule 5	LrLs or (LrLs)⁻¹: Add an inverter on the Scan enable
rule 6	ScSt: set TI to Vss and connect TE to Reset terminal
rule 7	ScRst: set TI to Vdd and connect TE to Set terminal
rule 8	ScRst(Ls⁻¹): set TI to Vdd and connect TE to set terminal with an inverter
rule 9	ScSt(Lr⁻¹): set TI to Vss and connect TE to reset terminal with an inverter
rule 10	ScStLrLs: set TI to Vss and connect TE to reset terminal with an inverter
rule 11	ScRstLrLs: set TI to Vdd and connect TE to set terminal with an inverter
rule 12	ScRstLr: set TI to Vdd and connect TE to set terminal
rule 13	ScStLs: set TI to Vss and connect TE to reset terminal
rule 14	Mu: connect D1 to TI and connect SEL to TE terminal
rule 15	Mu(LrLs)⁻¹: connect D0 to TI and connect SEL to TE terminal
rule 16	MuScSt: set D1 to Vss and connect SEL to Reset terminal
rule 17	MuScRst: set D1 to Vdd and connect SEL to set terminal
rule 18	MuScRst(Ls⁻¹): set D0 to Vdd and connect SEL to set terminal
rule 19	MuScSt(Lr⁻¹): set D0 to Vss and connect SEL to set terminal
rule 20	Mu⁻¹: connect D1 to TI, SEL to TE
rule 21	(Mu⁻¹)LsLr: connect D0 to TI, SEL to TE

FIG. 6

Inference	
Rst	infer a Reset active high
RstLr	infer a Reset active low
St	infer a Set active high
StLs	infer a Set active low
ScStRst	infer a Scan active high
ScStLsRstLr	infer a Scan active low
MuScStRst	infer a Mux
Re	infer a Recirculating active high
ReLre	infer a Recirculating active low
T	infer a Toggle element

FIG. 7

row/column	Rst	RstLr	St	StLs	ScStRst	ScStLsRstLr	MuScStRst	Re	ReLre	T
Rst	T1	T2	-----	-----	-----	-----	-----	-----	-----	-----
RstLr	T2	T1	-----	-----	-----	-----	-----	-----	-----	-----
St	-----	-----	T1	T3	-----	-----	-----	-----	-----	-----
StLs	-----	-----	T3	T1	-----	-----	-----	-----	-----	-----
ScStRst	T6	T9	T7	T8	T1	T5	T20	-----	-----	-----
ScStLsRstLr	T10	T13	T11	T12	T5	T1	T21	-----	-----	-----
MuScStRst	T16	T19	T17	T18	T14	T15	T1	-----	-----	-----
Re	-----	-----	-----	-----	-----	-----	-----	T1	T4	-----
ReLre	-----	-----	-----	-----	-----	-----	-----	T4	T1	-----
T	-----	-----	-----	-----	-----	-----	-----	-----	-----	T1

FIG. 8

66700T-8T05T460

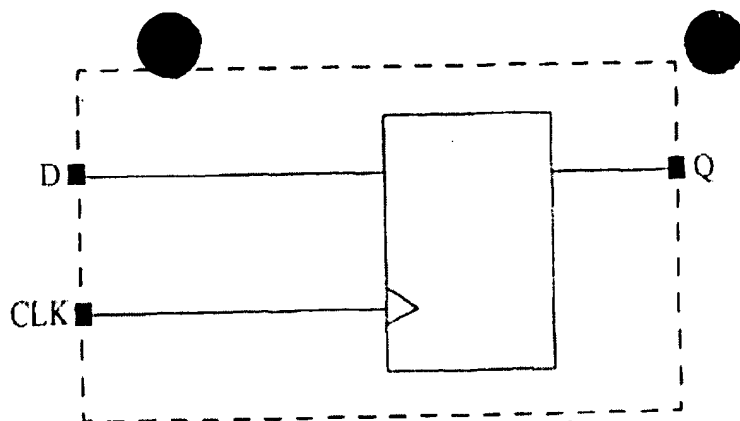


FIG. 9

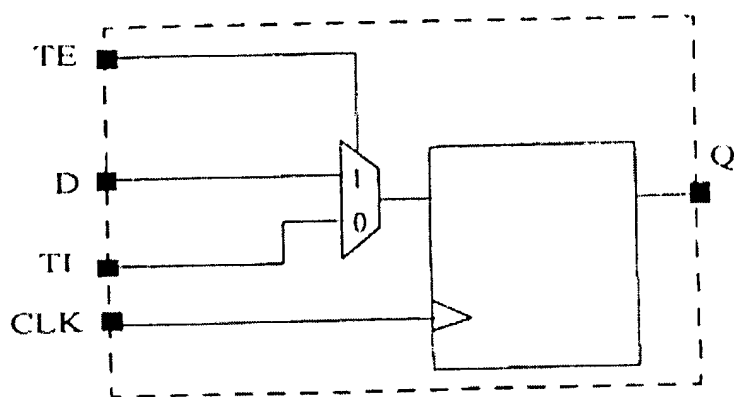


FIG. 10

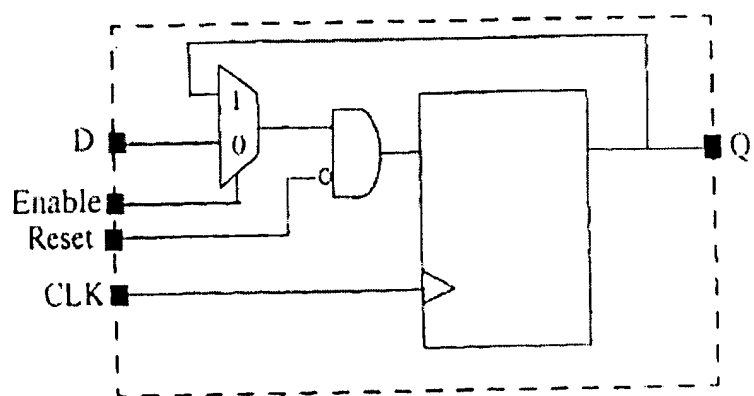


FIG. 11